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Date: September 11, 2007 /Kimberly Webb/
Kimberly Webb

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:			
Applicant(s):	Fred C. Tramm *et al.*	Examiner:	Eva Y. Zheng
Serial No:	10/611,525	Art Unit:	2611
Filing Date:	July 1, 2003		

Title: SYSTEMS AND METHOD FOR LOW LOSS MONOLITHIC EXTREMELY HIGH FREQUENCY QUADRA-PHASE SHIFT KEY MODULATION

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

Applicant submits this brief in connection with an appeal of the above-identified patent application. A credit card payment form is filed concurrently herewith in connection with all fees due regarding this appeal brief. In the event any additional fees may be due and/or are not covered by the credit card, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1063 [TRWP122US].

I. Real Party in Interest (37 C.F.R. §41.37(c)(1)(i))

The real party in interest in the present appeal is Northrop Grumman, the assignee of the present application.

II. Related Appeals and Interferences (37 C.F.R. §41.37(c)(1)(ii))

Appellants, appellants' legal representative, and/or the assignee of the present application are not aware of any appeals or interferences which may be related to, will directly affect, or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims (37 C.F.R. §41.37(c)(1)(iii))

Claims 1-30 stand rejected by the Examiner. The rejection of claims 1-30 is being appealed.

IV. Status of Amendments (37 C.F.R. §41.37(c)(1)(iv))

Appellants' legal representative submitted amendments to the Specification in a Reply to the Final Office Action to include government contract clauses. No amendments to the claims were submitted after the Final Office Action. (*See* Applicants' Reply to Final Office Action dated May 17, 2007).

V. Summary of Claimed Subject Matter (37 C.F.R. §41.37(c)(1)(v))

A. Independent Claim 1

Independent claim 1 recites a signal processing system, comprising: a component that receives an antenna pointing signal; and a monolithic shift key (SK) modulation component, incorporating at least one positive-intrinsic-negative (PIN) diode, the PIN diode switch the signal through a plurality of phase shifting paths to introduce a plurality of phase shifts to the signal based on one of number or combination of the plurality of phase shifting paths. (*See e.g.*, ¶ 0007, ll. 2-6; ¶ 0009, ll. 1-5; ¶ 0010, ll. 1-10; ¶ 0028, ll.1-10; ¶ 0032, ll.1-3; ¶ 0034; ¶ 0042; ¶ 0044; ¶ 0045; *See generally* Figs. 1, and 3-6).

B. Independent Claim 18

Independent claim 18 recites a transceiver, comprising: a transceiving component that obtains and conveys signals associated with antenna auto-tracking; and a phase shifting component that phase shifts the signals *via* a low loss monolithic quadra-phase shift key (QPSK) modulator, the QPSK modulator utilizes at least one positive-intrinsic-negative (PIN) diode to introduce a plurality of phase shifts by switching the signals through a plurality of phase shifting paths. (*See e.g.*, ¶ 0007, ll. 2-6; ¶ 0009, ll. 1-5; ¶ 0010, ll. 1-10; ¶ 0028, ll.1-10; ¶ 0032, ll.1-3; ¶ 0034; ¶ 0042; ¶ 0044; ¶ 0045; *See generally* Figs. 1, and 3-6).

C. Independent Claim 24

Independent claim 24 recites a method to process signals that facilitate antenna auto-tracking, comprising: receiving a signal; and modulating the signal *via* a positive-intrinsic-negative (PIN) diode quadra-phase shift key (QPSK) integrated circuit (IC) that incorporates at least one PIN diode to switch the signal through a plurality of phase shifting paths to introduce a plurality of phase shifts based on one of number and combination of the plurality of phase shifting paths. (*See e.g.*, ¶ 0007, ll. 2-6; ¶ 0009, ll. 1-5; ¶ 0010, ll. 1-10; ¶ 0028, ll.1-10; ¶ 0032, ll.1-3; ¶ 0034; ¶ 0042; ¶ 0044; ¶ 0045; *See generally* Figs. 1, and 3-6).

D. Independent Claim 30

Independent claim 30 recites a communications system, comprising: means for receiving a signal; means for utilizing at least one positive-intrinsic-negative (PIN) diode to switch the signal through a plurality of phase shifting paths to introduce a plurality of phase shifts based on one of number and combination of the plurality of phase shifting paths; and means for quadra-phase shift key modulating the signal, wherein the modulated signal is employed to facilitate antenna auto-tracking. (*See e.g.*, ¶ 0007, ll. 2-6; ¶ 0009, ll. 1-5; ¶ 0010, ll. 1-10; ¶ 0028, ll.1-10; ¶ 0032, ll.1-3; ¶ 0034; ¶ 0042; ¶ 0044; ¶ 0045; *See generally* Figs. 1, and 3-6).

VI. Grounds of Rejection to be Reviewed (37 C.F.R. §41.37(c)(1)(vi))

A. Claims 1-8, 10-15 and 18-30 are unpatentable under 35 U.S.C. §103(a) over Reinhardt *et al.* (US Patent 5,541,607) in view of Hong *et al.* (US Patent 6,281,838).

B. Claim 9 is unpatentable under 35 U.S.C. §103(a) over Reinhardt *et al.*(US Patent 5,541,607) in view of Hong *et al.* (US Patent 6,281,838) further in view of Taft *et al.* (US Patent 7,030,824).

C. Claim 16 is unpatentable under 35 U.S.C. §103(a) over Reinhardt (US Patent 5,541,607) in view of Hong *et al.* (US Patent 6,281,838) further in view of Mano *et al.* (US Patent 6,778,586).

D. Claim17 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Reinhardt *et al.* (US Patent 5,541,607) in view of Hong *et al.* (US Patent 6,281,838) further in view of Stiles *et al.* (US Patent 3,768,050).

VII. Argument (37 C.F.R. §41.37(c)(1)(vii))

A. Rejection of Claims 1-8, 10-15 and 18-30 Under 35 U.S.C. §103(a)

Claims 1-8, 10-15 and 18-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Reinhardt *et al.* (US Patent 5,541,607) in view of Hong *et al.* (US Patent 6,281,838). Reversal of this rejection is respectfully requested for at least the following reasons. Reinhardt *et al.* and Hong *et al.*, either alone or in combination, fail to teach or suggest each and every limitation set forth in the subject claims.

> To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) ***must teach or suggest all the claim limitations.*** *See* MPEP §706.02(j). The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *See In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Applicants' claimed invention relates generally to systems and methods that facilitate signal modulation, and in particular to a positive-intrinsic-negative (PIN) diode switch based delay line quadra-phase shift key (QPSK) modulator based on microwave monolithic integrated circuit (MMIC) technology. It should be noted that through the use of MMIC technology these phase shifters can be consistently fabricated on a single chip for extremely high frequency operation. Furthermore, utilizing MMIC technology to create a PIN Diode switch based delay line QPSK modulator can reduce the footprint and assembly cost, and increase performance *via* mitigating parasitic reactance. In particular, independent claim 1 in part recites *a component that receives an antenna pointing signal; and a* ***monolithic*** *shift key (SK)* ***modulation*** *component incorporating at least one positive-intrinsic-negative* ***(PIN) diode*** ... Similar limitations of "a ***phase shifting component***... *via a low loss* ***monolithic*** *quadra-phase shift key (QPSK) modulator, the QPSK modulator utilizes at least one positive-intrinsic-negative* ***(PIN) diode,***" "***modulating*** *the signal via a positive-intrinsic-negative* ***(PIN) diode*** *quadra-phase shift key (QPSK) integrated circuit (IC),*" and "*means for utilizing at least one positive-intrinsic-negative* ***(PIN) diode*** *to* ***switch the signal,***" are recited in independent claims 18, 24, and 30 respectively. Reinhardt *et al.* fails to disclose or suggest such aspects of the invention as claimed.

Reinhardt *et al.* merely discloses a system and method for polar digital beamforming, where complex weighing signals can be generated by summing a sequence of complex multiplications or by simply inverting the real and imaginary components of the weighting signal for particular modulation schemes. Reinhardt *et al.* discloses a multiple-beam phased array antenna which digitally generates pointing and modulation information, and utilizes a simple polar architecture to implement polar digital beamforming. Reinhardt *et al.*, further discloses utilizing phasors, attenuators, and previously developed digital Application Specific Integrated Circuits (ASICs) to implement polar digital beamforming. (*See*, column 2, lines 52-67).

In the Final Office Action (dated May 17, 2007), the Examiner argues that Reinhardt *et al.* discloses a monolithic shift key modulation component (ASIC column 2, lines 65-67, column 6, lines 25-60). Applicants' representative respectfully disagrees. As was stated in the applicants' Reply to Final Office Action, and is reiterated herein, Reinhardt *et al.* merely discloses the use of *previously developed* phasors, attenuators, Application Specific Integrated Circuits (ASICs) and fails to disclose or suggest utilizing monolithic microwave integrated circuit (MMIC) technology to create a ***monolithic*** shift key (SK) modulation component,

incorporating at least one positive-intrinsic-negative (PIN) diode. The Examiner is reminded that a mere reference to the use of previously developed Integrated Circuits (e.g. ASIC) in a particular system does not suggest the development and/or construction (fabrication) of the system using that particular technology (e.g. MMIC technology).

In the Advisory Action (dated June 26, 2007), the Examiner argues that MMIC and ASIC, though different in name, are similar technologies and are used interchangeably. While applicants' representative agrees with the Examiner's argument that MMIC and ASIC are similar technologies, Reinhardt *et al.* fails to disclose or suggest the use of any of these technologies for the development and/or construction (monolithic fabrication) of the shift key modulation component. As mentioned *supra,* Reinhardt *et al.* merely uses previously developed ASIC's along with modulation component. Nowhere does Reinhardt *et al.* disclose or suggest that the shift key modulation component is ***monolithic,*** wherein the modulation component is constructed and/or developed (fabricated) using any of the integrated circuit (e.g., MMIC, ASIC) technologies. On the other hand, the claimed subject matter clearly recites *a* ***monolithic shift key (SK) modulation*** *component, incorporating at least one positive-intrinsic-negative (PIN) diode.* To this end, the Specification discloses the use of phase shifting components, which can include PIN diode switched delay lines, to generate a four phase states for QPSK modulation. The Specification further discloses that MMIC technology can be employed to construct the phase shifting components and the QPSK modulator. (*See,* Specification, paragraph 0050).

Independent claim 1 (and similarly independent claims 18, 24, and 30) further recites: "the PIN diode switch the signal through a plurality of phase shifting paths to introduce a plurality of phase shifts to the signal based on one of number or combination of the plurality of phase shifting paths." The Examiner concedes that Reinhardt *et al.* does not disclose a "*shift key (SK) modulation…incorporating …**a PIN diode**…plurality of phase shifting paths…,*" and offers Hong *et al.* to cure this deficiency. The Examiner states that Hong *et al.* discloses "a select line phase shifter using micro electromechanical system ***(MEMS), wherein PIN switches are used*** …plurality of phase shifts." Applicants' representative respectfully disagrees. One of ordinary skill in the art will understand that MEMS and PINS are two very different devices and MEMS switches do not use PIN switches. MEMS are micro electromechanical systems. As the name suggests, MEMS are formed by the integration of mechanical and electrical elements. Hong *et al.* discloses the following about a MEMS switch:

> "MEMS switch is formed on a semi-insulating substrate and includes a cantilever arm that is affixed to the substrate and extends over a ground line, and a gapped signal line formed by metal microstrips on the substrate. An electrical contact is formed on the bottom of the cantilever arm positioned above and facing the gap in the signal line. A top electrode on the cantilever arm forms a capacitor structure above the ground line on the substrate. The switch is actuated by application of a voltage to the top electrode. With voltage applied, electrostatic forces attract the capacitor structure toward the ground line, thereby causing the metal contact to close the gap in the signal line and thus close the switch." (*See*, column 3, lines 9-21).

From the foregoing excerpts, it is readily apparent that MEMS switch does not use PIN diode switches. Rather a MEMS switch uses electrostatic forces to provide ***mechanical movement*** to achieve short circuit or open circuit in a signal line, and provide the functionality of switching. Therefore, it is readily apparent that the Examiner incorrectly interprets that Hong *et al.* discloses a MEMS switches, wherein PIN switches are used.

Additionally, in the Final Office Action (dated May 17, 2007), the Examiner argues that Hong *et al.* discloses: "PIN diode switches are used through a plurality of phase shift paths to introduce a plurality of phase shifts (Fig.3; Col 4, L 29-67). The loss and distortion experienced by the transmission signal is significantly reduced (Col 2, L52-54)." Applicants' representative respectfully disagrees. Nowhere does Hong *et al.* disclose or suggest that by using PIN diode switches, through a plurality of phase shift paths, the loss and distortion experienced by the transmission signal is signal is significantly reduced. In fact, Hong *et al.* discloses that ***PIN diode switches suffer from insertion loss*** dominated by the resistive loss of the signal line. (*See*, column 2, lines 23-32). Hong *et al.* merely discloses using more delay lines per stage (preferably three as opposed to two) to provide improved insertion loss and isolation characteristics. Hong *et al.* fails to discloses or suggest "*a* ***monolithic shift key (SK) modulation*** *component,* ***incorporating at least one positive-intrinsic-negative (PIN) diode****, the PIN diode switch the signal through a plurality of phase shifting paths..."* as recited in the claimed subject matter.

In view of at least the foregoing, it is readily apparent that and Reinhardt *et al.* and Hong *et al.*, either alone or in combination, do not disclose or suggest the claimed invention as recited

in independent claims 1, 18, 24, and 30 (and claims which depend there from). Therefore, reversal of this rejection is requested.

B. Rejection of Claim 9 Under 35 U.S.C. §103(a)

Claim 9 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Reinhardt *et al.*(US Patent 5,541,607) in view of Hong *et al.* (US Patent 6,281,838) further in view of Taft *et al.* (US Patent 7,030,824). Reversal of this rejection is respectfully requested for at least the following reasons. Reinhardt *et al.*, Hong *et al.* and Taft *et al.*, individually or in combination, do not teach or suggest each and every element set forth in the subject claims. In particular, Taft *et al.* does not make up for the aforementioned deficiencies of Reinhardt *et al.* and Hong *et al.* with respect to independent claim 1 (which claim 9 depends from). Therefore, the claimed invention as recited in claim 9 is not obvious over the combination of Reinhardt *et al.*, Hong *et al.* and Taft *et al.* Thus, it is respectfully submitted that this rejection be reversed.

C. Rejection of Claim 16 Under 35 U.S.C. §103(a)

Claim 16 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Reinhardt (US Patent 5,541,607) in view of Hong *et al.* (US Patent 6,281,838) further in view of Mano *et al.* (US Patent 6,778,586). Reversal of this rejection is respectfully requested for at least the following reasons. Reinhardt *et al.*, Hong *et al.* and Mano *et al.*, individually or in combination, do not teach or suggest each and every element set forth in the subject claims. In particular, Mano *et al.* does not make up for the aforementioned deficiencies of Reinhardt *et al.* and Hong *et al.* with respect to independent claim 1 (which claim 16 depends from). Therefore, the claimed invention as recited in claim 16 is not obvious over the combination of Reinhardt *et al.*, Hong *et al.* and Mano *et al.* Accordingly, reversal of this rejection is requested.

D. Rejection of Claim 17 Under 35 U.S.C. §103(a)

Claim 17 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Reinhardt *et al.* (US Patent 5,541,607) in view of Hong *et al.* (US Patent 6,281,838) further in view of Stiles *et al.* (US Patent 3,768,050). Reversal of this rejection is respectfully requested for at least the following reasons. Reinhardt *et al.*, Hong *et al.* and Stiles *et al.*, individually or in combination, do not teach or suggest each and every element set forth in the subject claims. In

particular, Stiles *et al.* does not make up for the aforementioned deficiencies of Reinhardt *et al.* and Hong *et al.* with respect to independent claim 1 (which claim 17 depends from). Therefore, the claimed invention as recited in claim 17 is not obvious over the combination of Reinhardt *et al.*, Hong *et al.* and Stiles *et al.* Thus, it is respectfully submitted that this rejection be reversed.

E. Conclusion

For at least the above reasons, the claims currently under consideration are believed to be patentable over the cited references. Accordingly, it is respectfully requested that the rejections of claims 1-30 be reversed.

If any additional fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [TRWP122US].

Respectfully submitted,
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VIII. Claims Appendix (37 C.F.R. §41.37(c)(1)(viii))

1. A signal processing system, comprising:

a component that receives an antenna pointing signal; and

a monolithic shift key (SK) modulation component, incorporating at least one positive-intrinsic-negative (PIN) diode, the PIN diode switch the signal through a plurality of phase shifting paths to introduce a plurality of phase shifts to the signal based on one of number or combination of the plurality of phase shifting paths.

2. The system of claim 1, the SK modulation component employing one or more binary phase shifters.

3. The system of claim 2, the respective binary phase shifters comprising multiple phase shifting paths in series to introduce a plurality of phase shifts based on the number of paths.

4. The system of claim 2, the binary phase shifters employed as a quadra-phase (QPSK) modulator to generate four phase shifts for the signal.

5. The system of claim 2, respective binary shifters comprising paths constructed in accordance with an equivalent electrical length that corresponds to a desired phase shift.

6. The system of claim 1, the SK modulation component employing one or more reflective phase shifters.

7. The system of claim 6, respective reflective phase shifters comprising two phase shifting sections, wherein respective phase shifting sections comprise a hybrid coupler and two PIN diode switches.

8. The system of claim 6, respective reflective phase shifters configured to generate at least a 90-degree phase shift and a 180-degrees phase shift *via* changing termination impedance state *via* the PIN diodes, wherein the 90 and 180 degree phase shifts are employed in connection to modulate the signal through four phase states.

9. The system of claim 1, the SK modulation component employing a hybrid reflective phase shifter comprising a binary phase shifter and a reflective phase shifter.

10. The system of claim 1, the SK modulation component employing a switched filter phase shifter that can be tuned for a particular phase shift over a plurality of frequencies.

11. The system of claim 10, the switched filter phase shifter comprising two parallel phase shifting networks in series, wherein respective networks provide two phase states, and coupling the networks provides for four phase states.

12. The system of claim 1, the SK modulation component configured as one of an amplitude shift key (ASK), a frequency shift key (FSK), a phase shift key (PSK), or a quadra-phase shift key (QPSK) modulator.

13. The system of claim 1, the monolithic SK modulation component constructed from microwave monolithic integrated circuit (MMIC) technology.

14. The system of claim 1, employed in connection with a satellite, aircraft or spacecraft.

15. The system of claim 1, further comprising a DC bias component employed to affect the impedance state of the PIN diode.

16. The system of claim 1, further comprising a RF matching component employed to pass signals within a desired frequency band, maximize power transfer and filter signals associated with undesired frequencies.

17. The system of claim 1, further comprising a high Q RF short component employed to provide an RF short for DC lines.

18. A transceiver, comprising:

a transceiving component that obtains and conveys signals associated with antenna auto-tracking; and

a phase shifting component that phase shifts the signals *via* a low loss monolithic quadra-phase shift key (QPSK) modulator, the QPSK modulator utilizes at least one positive-intrinsic-negative (PIN) diode to introduce a plurality of phase shifts by switching the signals through a plurality of phase shifting paths.

19. The system of claim 18, the phase shifting component employing one of a binary phase shifter, a reflective phase shifter, a hybrid phase shifter or a switched filter phase shifter.

20. The system of claim 18, the phase shifting component comprising PIN diode switches.

21. The system of claim 18, employed in connection with a satellite, aircraft or spacecraft.

22. The system of claim 18, the monolithic QPSK modulator constructed from microwave monolithic integrated circuit (MMIC) technology.

23. The system of claim 18, further comprising a diagnostic component to verify and facilitate trouble shooting the phase shifting component.

24. A method to process signals that facilitate antenna auto-tracking, comprising:

receiving a signal; and

modulating the signal *via* a positive-intrinsic-negative (PIN) diode quadra-phase shift key (QPSK) integrated circuit (IC) that incorporates at least one PIN diode to switch the signal through a plurality of phase shifting paths to introduce a plurality of phase shifts based on one of number and combination of the plurality of phase shifting paths.

25. The method of claim 24, the PIN diode QPSK IC fabricated based on microwave monolithic integrated circuit (MMIC) technology.

26. The method of claim 24, the PIN diode employed as a switch to switch between reference and delay lines.

27. The method of claim 24, further comprising one or more of filtering signal noise, amplifying the signal, low pass filtering the signal, high pass filtering the signal, band pass filtering the signal, encrypting the signal, decrypting the signal, encoding the signal, or decoding the signal.

28. The method of claim 24, further comprising employing one of binary, reflective, hybrid, or switched filter based phase shifting.

29. A satellite, aircraft or spacecraft employing the method of claim 24.

30. A communications system, comprising:

means for receiving a signal;

means for utilizing at least one positive-intrinsic-negative (PIN) diode to switch the signal through a plurality of phase shifting paths to introduce a plurality of phase shifts based on one of number and combination of the plurality of phase shifting paths; and

means for quadra-phase shift key modulating the signal, wherein the modulated signal is employed to facilitate antenna auto-tracking.

IX. Evidence Appendix (37 C.F.R. §41.37(c)(1)(ix))

None.

X. Related Proceedings Appendix (37 C.F.R. §41.37(c)(1)(x))

None.